The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously presented) A re-writable memory comprising:

a plurality of x-direction conductive layers, each conductive layer being patterned to form conductive array lines in a first direction;

a plurality of y-direction conductive layers, each conductive layer being patterned to form conductive array lines in a second direction orthogonal to the first direction; and

a plurality of memory cell arrays, each one defined in-between an x-direction conductive layer and a y-direction conductive layer, each memory cell array being accessible for reading or writing through selection of

an x-direction conductive layer operably connected to the memory cell array; and

a y-direction conductive layer operably connected to the memory cell array;

wherein the selection of only one conductive layer is not sufficient to access a memory cell array for either reading or writing.

2. (Previously presented) The re-writable memory of claim 1, wherein:

the selection of one memory cell array can cause multiple x-direction conductive layers to be selected.

3. (Original) The re-writable memory of claim 2, wherein:

the multiple x-direction conductive layers that are selected when some memory cell arrays are selected are electrically coupled.

4. (Original) The re-writable memory of claim 3, wherein:

thrus are used to electrically couple the multiple x-direction conductive layers.

5. (Original) The re-writable memory of claim 1, further comprising:

a first set of x-direction selection circuitry operably connected to a first portion of the plurality of x-direction conductive array layers;

a second set of x-direction selection circuitry operably connected to a remaining portion of the plurality of x-direction conductive array layers; and

a plurality of sets of y-direction selection circuitry, each set of y-direction selection circuitry operably connected to one of the y-direction conductive array layers.

6. (Original) The re-writable memory of claim 5, wherein:

there are at least two x-direction conductive array layers in the first portion.

7. (Original) The re-writable memory of claim 6, wherein:

the number of x-direction conductive array layers in the first portion and the number of x-direction conductive array layers in the remaining portion are within one of each other.

8. (Original) The re-writable memory of claim 7, wherein:

there are three x-direction conductive array layers, whereby two x-direction conductive array layers are in the first portion and the remaining x-direction conductive array layer is in the second portion;

there are two y-direction conductive array layers, whereby each y-direction conductive array line is operably connected to a set of y-direction selection circuitry; and

there are four memory cell arrays.

9. (Original) The re-writable memory of claim 7, wherein:

there are five x-direction conductive array layers, whereby three x-direction conductive array layers are in the first portion and the remaining two x-direction conductive array layers are in the second portion;

there are four y-direction conductive array layers, whereby each y-direction conductive array line is operably connected to a set of y-direction selection circuitry; and

there are eight memory cell arrays.

10. (Original) A re-writable memory comprising:

a plurality of conductive line arrays;

a plurality of driver sets that drive the conductive line arrays, each driver set using a selection logic to drive the conductive line arrays, wherein at least two conductive line arrays are driven by the same selection logic; and

a plurality of memory cell arrays, each memory cell array being in electrical contact with two conductive line arrays and requiring both of those conductive line arrays to be driven by

their appropriate driver sets in order to access the memory cell array for reading and writing purposes, whereby a memory cell array cannot be read from or written to by a single conductive line array being driven.

11. (Original) The re-writable memory of claim 10, wherein:

the at least two conductive line arrays that are driven by the same selection logic are driven by the same driver set.

12. (Original) The re-writable memory of claim 10, wherein:

there are five conductive line arrays and four memory cell array.

13. (Original) The re-writable memory of claim 12, wherein:

there are four driver sets, one of the driver sets driving two of the conductive line arrays.

14. (Original) The re-writable memory of claim 12, wherein:

there are five driver sets, two of the driver sets having the same selection logic.

15. (Original) The re-writable memory of claim 10, wherein:

there are nine conductive line arrays and eight memory cell arrays.

16. (Original) The re-writable memory of claim 15, wherein:

there are six driver sets, one of the driver sets driving two of the conductive line arrays and another of the driver sets driving three of the conductive line arrays.

17. (Original) The re-writable memory of claim 15, wherein:

there are nine driver sets,

two of the driver sets having a first selection logic; and

three of the driver sets having a second selection logic.

18. (Original) A re-writable memory comprising:

at least three x-direction conductive layers, each conductive layer being patterned to form conductive array lines in a first direction, wherein at least two x-direction conductive layers are driven by the same logic;

at least two y-direction conductive layers, each conductive layer being patterned to form conductive array lines in a second direction orthogonal to the first direction;

at least four memory cell arrays, each memory cell array being operably connected to one x-direction conductive layer and one y-direction conductive layer.

19. (Original) The re-writable memory of claim 18, wherein:

a plurality of resistive memory elements are used in each memory cell array.

20. (Original) The re-writable memory of claim 19, wherein:

the resistive memory elements are formed from conductive metal oxides.

21. (Original) The re-writable memory of claim 20, wherein:

the re-writable is accessed during a standard cycle, the standard cycle being used for either reading or writing.

22. (Original) The re-writable memory of claim 21, wherein:

the standard cycle is less than 100 ns.

23. (Original) The re-writable memory of claim 18, wherein:

writing to a single memory cell can be accomplished without disturbing other memory cells in the memory cell array, whereby the re-writable memory is byte re-writable and not block writable.

24. (Previously Presented) A re-writable memory comprising:

a plurality of x-direction conductive layers, each conductive layer being patterned to form conductive array lines in a first direction;

a least one y-direction conductive layer, each conductive layer being patterned to form conductive array lines in a second direction orthogonal to the first direction; and

a plurality of memory cell arrays, each one defined in-between an x-direction conductive layer and a y-direction conductive layer, each memory cell array being accessible for reading or writing through selection of

an x-direction conductive layer operably connected to the memory cell array; and

a y-direction conductive layer operably connected to the memory cell array,

wherein each memory cell is defined by at least a memory plug placed at or near the intersection of one x-direction conductive array line and one y-direction conductive array line.

25. (Original) The re-writable memory of claim 24, wherein:

the memory plugs exhibit a non-linear resistive characteristic.

26. (Original) The re-writable memory of claim 25, wherein:

the memory plug includes a conductive metal oxide.